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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/904,663	07/16/2001	Mikio Ohtaki	KAN 120D1	7934

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EXAMINER	
HOLLINGTON, JERMELE M	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 04/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/904,663	OHTAKI, MIKIO	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-27 and 42-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-27 and 42-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/434,490.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 21-27 and 42-52 have been considered but are moot in view of the new ground(s) of rejection given below.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 21-27 and 42-52 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claims 21, 42-44 and 51-52, the claim recites: "...the back or second surface of the wafer exposed to convective air in the burn-in apparatus..." The specification does not in a clear, concise and full description describe the above claim limitation. On page 23, lines 25-30, it describes a ventilating through holes in the hold pate to help circulate air to the expose wafer. However, it does not describe that the air is being exposed to the back surface of the wafer as claimed.

For examination purposes, the examiner is not giving patentable weight to the limitation "the back surface of the wafer exposed to convective air" until further explanation is given of

this limitation in the claim. Since claims 22-27 depend off of claim 21 and claims 45-52 depend off of claim 44, they are also rejected.

Regarding claims 24, 26, 47 and 49, the claim recites: "...disposing over the back or second surface of the wafer a holding plate having a through hole..." The specification does not in a clear, concise and full description describe the above claim limitation. On page 23, lines 25-30, it describes a ventilating through holes in the hold pate to help circulate air to the expose wafer. However, it does not describe that the holding plate is being dispose over the back surface of the wafer as claimed.

For examination purposes, the examiner is not giving patentable weight to the limitation "the back surface of the wafer" until further explanation is given of this limitation in the claim. Since claim 42 depends off of claim 24, claim 43 depends off of claim 26, claim 51 depends off of claim 47 and claim 52 depends off of claim 49, they are also rejected.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 21-27 and 44-50 are rejected under 35 U.S.C. 102(b) as being anticipated by Wood et al (5663654).

Regarding claim 21,Wood et al discloses [see Fig. 4] a method of manufacturing semiconductor devices comprising providing a semiconductor wafer (wafer 30) with a front

surface (top surface of wafer 30) inherently having a plurality of circuit elements (not shown in the Figure) formed thereon, where the semiconductor wafer (30) has a back surface (bottom of wafer 30) opposite to the front surface (top surface of wafer 30), forming on the front surface a plurality of electrodes (not shown but see col. 3, lines 57-60 or col. 6, lines 7-11) connected with the circuit elements, inserting the wafer (30) into a burn-in apparatus (represented as burn-in tst fixture) [see also col. 6, lines 30-34], wherein the semiconductor wafer (30) is positioned in a positioning plate (wafer cavity plate 11') having a hole (wafer receiving cavity 17'), the hole (17) being formed in a shaped to an outer shape of the semiconductor wafer [see Fig. 4 for details], testing the plurality of circuit elements [not shown] for electrical functions in the burn-in apparatus (burn-in test fixture) through the plurality of electrodes (16) [see col. 1, lines 13-17 and col. 3, lines 37-39] and dividing the wafer (30) into the plurality of semiconductor devices [see col.5, lines 43-44].

Regarding claims 22, Wood et al disclose dividing the wafer after testing [see col. 5, lines 43-44].

Regarding claims 23 and 25, Wood et al disclose mounting the wafer (30) on a circuit board (main plate portion 21') with an elastic sheet or film (substrate 63) [see col. 5, lines 7-28 and col. 6, lines 45-51 interposed there between [see Fig. 4] including electrically connecting wiring circuit (not number in the Figure but known as circuit traces) [see col. 6, lines 52-57] on the circuit board (2") to the electrodes on the wafer (30) through conductive elastic portions or bump electrodes in the elastic sheet or film (63) [see also col. 5, lines 15-19].

Regarding claims 24 and 26, Wood et al disclose disposing over the wafer (30) a holding plate (support plate 12') having a through hole (dowel receiving cavities 28') and pressing the wafer (30) on the circuit board (21') with the holding plate (12').

Regarding claim 27, Wood et al disclose inherently forming a plurality of solder balls as the electrodes (17) [see col. 3, lines 57-60].

Regarding claim 44, Wood et al disclose [see Fig. 4] a method of manufacturing semiconductor devices comprising preparing a semiconductor wafer (wafer 30) with a first surface (top surface of wafer 30) and a second surface (bottom surface of wafer 30), the second surface being opposite to the first surface, wherein the first surface has a plurality of circuit elements [not shown] formed thereon [see column 3, lines 57-60 and col. 6, lines 4-9], forming a plurality of electrodes on the first surface [see column 3, lines 57-60 and col. 6, lines 4-9], the electrodes (16) being connected to the circuit elements [see column 6 lines 30-31], inserting the wafer (30) into a burn-in apparatus (represented as burn-in test fixture) [see col. 3, lines 37-39], wherein the semiconductor wafer (30) is positioned in a positioning plate (wafer cavity plate 11') having a hole (wafer receiving cavity 17'), the hole (17) being formed in a shaped to an outer shape of the semiconductor wafer [see Fig. 4 for details], testing the plurality of circuit elements [not shown] for electrical functions in the burn-in apparatus (burn-in test fixture) through the plurality of electrodes (16) [see col. 1, lines 13-17 and col. 3, lines 37-39] and dividing the wafer (30) into the plurality of semiconductor devices [see col.5, lines 43-44].

Regarding claims 45, Wood et al disclose dividing the wafer after testing [see col. 5, lines 43-44].

Regarding claims 46 and 48, Wood et al disclose mounting the wafer (30) on a circuit board (main plate portion 21') with an elastic sheet or film (substrate 63) [see col. 5, lines 7-28 and col. 6, lines 45-51 interposed there between [see Fig. 4] including electrically connecting wiring circuit (not number in the Figure but known as circuit traces) [see col. 6, lines 52-57] on the circuit board (2") to the electrodes on the wafer (30) through conductive elastic portions or bump electrodes in the elastic sheet or film (63) [see also col. 5, lines 15-19].

Regarding claims 47 and 49, Wood et al disclose [see Figs. 1A-2B] disposing over the second surface [top surface using Figs. 1A-2B] of the wafer (30) a holding plate (support plate 12 in Fig. 2B) having a through hole (dowel receiving cavities 28) and pressing the wafer (30) on the circuit board (21) with the holding plate (12).

Regarding claim 50, Wood et al disclose inherently forming a plurality of solder balls as the electrodes (17) [see col. 3, lines 57-60].

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Gross (5206181), Devereaux et al (5279975), Tsujide et al (5532610), Tuckerman et al (5541524), Mignardi et al (5597767), Seki (5986282) and Pierce (6440771) disclose a method and apparatus for testing wafers.

7. The applicant argues: "The Examiner's §112, first paragraph, rejection is respectfully traversed...What the Examiner fails to note, as disclosed in Figures 17, and in detail in Figure 18, and discussed on page 24, lines 17-31...Thus, when the application is considered as a whole, it is clear that the limitations...are, in fact, disclosed in a manner so as to reasonably convey to

one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention..."

The examiner will like to thank the applicant for providing additional information regarding the use of the limitation "back surface of the wafer." However, reviewing the cited portions by the applicant, the examiner still finds as not persuasive. In reviewing page 24, lines 17-31 and Figs. 17-18, it seems impossible for the back surface of the wafer to be exposed to air as claimed. On page 24, lines 21-23, it states: *"The pressure from the holding plate 309 is distributed evenly and correctly to the wafer to be measured 401by the buffer member 313 provided at the holding plate 309."* The buffer member 313, which is not disclosed in Fig. 13 or page 23, lines 25-30, is covering the holding plate 309, which in turn coves the ventilating through holes 309, shown in Fig. 13. With the ventilating through holes 309 cover by the buffer, it is not possible for the back surface of the wafer exposed to convective air as claimed. Form the examiner's view, the only way convective air could be expose to the wafer, base on Figs. 17-18, is through film 305, which is connected to the front surface of the wafer. Furthermore, page 23, lines 25-27, it states: "A plurality of ventilating through holes 309b are formed at the holding plate 309. This makes it possible to exposed the wafer to be measured 401 to the air circulates through convection..." Base on the above statement, the specification does not disclose that it refers to the front or back of the wafer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (517) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Examiner
Art Unit 2829

JMH
March 23, 2004